43. The method of claim 26, wherein said first voltage is supplied from a first power supply and said second voltage is supplied from a second power supply, said first power supply and said second power supply being separate from one another.

44. The method of claim 33, wherein said first voltage is supplied from a first power supply and said second voltage is supplied from a second power supply, said first power supply and said second power supply being separate from one another.--

REMARKS

I. Introduction

In response to the pending rejection, Applicants have added new claims 39-44 so as to recite an additional feature of the present invention not previously claimed. Support for new claims 39-44 can be found, for example, in Fig. 1. No new matter has been added. For the reasons set forth below, Applicants respectfully traverse the pending rejections of the claims in view of the cited prior art.

In addition, Applicants have amended the Title of the invention in accordance with the Examiner's suggestion. The specification was amended to update the priority information.

Finally, it is noted that the Chinese, Korean and Taiwanese documents cited in the Information Disclosure Statement (IDS) filed on April 24, 2002 correspond to the publication of the corresponding foreign application of the priority application. Further, it appears that an Abstract of the present application was submitted along with the IDS filed on April 24, 2002 so as to serve as the English abstract of the three references noted by the Examiner. Accordingly, it is respectfully requested that the three

references be formally considered by the Examiner. It is noted that these references are only relative as prior art to the "new matter" contained in the instant application, and not to any portion of the present application that is supported in the priority document.

II. The Rejection Of Claims 1, 3, 5, 6, 20, 22, 24 And 25 Under 35 U.S.C. § 103

Claims 1, 3, 5, 6, 20, 22, 24 and 25 were rejected under 35 U.S.C. § 103 as being obvious over USP No. 5,672,541 to Booske in view of Wolf, Silicon Processing for the VLSI Era. Applicants respectfully traverse this rejection for the following reasons.

With regard to claims 1 and 20, which are the only independent claims contained in the foregoing rejection, both of these method claims recite the step of applying a first voltage to an impurity solid, such that it serves as a cathode (claim 1) or anode (claim 20) for the plasma. In the pending rejections, Booske is relied upon as disclosing this element of the method claims. However, it is respectfully submitted that this conclusion is incorrect. Booske does not appear to disclose applying any type of voltage to the impurity solid. As set forth on col. 9, lines 14-21, Booske discloses firing ions at the target 46 (i.e., impurity solid) by means of an ion source 44 in order to sputter the target material and form the thin layer 38. Indeed, the portion of Booske cited in the pending rejection, which is col. 7, lines 1-2, merely states that plasma surrounds the substrate 20 so as to accelerate ions which will impact the substrate 20. Thus, at a minimum, Booske fails to disclose the foregoing element of claims 1 and 20. It is noted that Wolf is not relied upon as curing the foregoing deficiency of Booske in the pending rejection.

Moreover, both independent claims 1 and 20 recite the step of sputtering the impurity impurity solid utilizing ions in the plasma. In contrast, the formation of thin layer

38 of Booske, which is formed by sputter deposition of the target 46 by an ion source, occurs prior to the generation of the plasma or the introduction of plasma into the chamber in the method disclosed by Booske. Col. 10, lines 13-29 of Booske makes this point clear. As such, Booske also fails to disclose this element of the methods recited by the independent claims 1 and 20. Wolf is not relied upon as curing this defect.

Accordingly, as each and every claim limitation must be disclosed or suggested by the cited prior art references in order to substantiate a rejection under 35 U.S.C. § 103 (*see*, M.P.E.P. § 2143.03), and the foregoing makes clear that Booske and Wolf fail to do so, it is submitted that claims 1 and 20 are patentable over both Booske and Wolf, taken alone or in combination with one another.

III. The Rejection Of Claims 7, 9, 11-13, 26, 28 And 30-32 Under 35 U.S.C. § 103

Claims 7, 9, 11-13, 26, 28 and 30-32 were rejected under 35 U.S.C. § 103 as being obvious over USP No. 5,672,541 to Booske in view of Wolf, Silicon Processing for the VLSI Era, and further in view of JP 05024976 to Nakagawa. Applicants respectfully traverse this rejection for the following reasons.

First, claims 7 and 26, which are the only independent claims in the foregoing rejection, recite the same elements as claims 1 and 20 discussed above in Section II. Accordingly, as the newly cited reference, Nakagawa, is not relied upon as curing the deficiencies of Booske noted above, it is respectfully submitted that claims 7 and 26 are patentable over the cited combination of prior art for the same reasons as set forth in Section II.

Further, as recited by claims 7 and 26 of the present invention a first voltage is applied to the impurity solid so as to allow the impurity solid to serve as a cathode for the plasma. Thus, the electrode applying the first voltage is a cathode. Further, a second voltage is applied to the semiconductor substrate so as to allow the substrate to serve as an anode for the plasma. Thus, the electrode applying the second voltage is an anode. In contrast, according to Nakagawa, a sample 105 is connected with an anode 103 and a target 109 is connected with a cathode 104. Thus, the relationship of the anode and cathode relative to the target and substrate are reversed in Nakagawa. Accordingly, Nakagawa fails to disclose this limitation recited by claims 7 and 26.

IV. The Rejection Of Claims 14, 16, 18, 19, 33, 35, 37 And 38 Under 35 U.S.C. § 103

Claims 14, 16, 18, 19, 33, 35, 37 and 38 were rejected under 35 U.S.C. § 103 as being obvious over USP No. 5,672,541 to Booske in view of Wolf, Silicon Processing for the VLSI Era, and further in view of JP 05024976 to Nakagawa and USP No. 4,596,645 to Stirn. Applicants respectfully traverse this rejection for the following reasons.

Claims 14 and 37, which are the only independent claims in the foregoing rejection, recite the same elements as claims 1 and 20 discussed above in Section II. Accordingly, as the newly cited reference, Stirn, is not relied upon as curing the deficiencies of Booske noted above, it is respectfully submitted that claims 14 and 37 are patentable over the cited combination of prior art for the same reasons as set forth in Section II.

Accordingly, it is respectfully requested that the rejection be withdrawn.

V. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as all pending independent claims are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

Further, it is noted that none of the prior art references appear to disclose the subject matter recited by newly added claims 39-44, which recite that the first voltage is supplied from a first power supply and that the second voltage is supplied from a second power supply, wherein the first power supply and the second power supply are separate from one another. As such, new claims 39-44 recite an additional distinct over the cited art.

VI. Conclusion

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an

Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 9/6/02

By: _____

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

The title has been amended as follows:

METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES BY SPUTTER-DOPING

IN THE SPECIFICATION:

Paragraph beginnning at page 1, line 3 has been amend as follows:

The application is a Continuation-In-Part of U.S. Patent Application Serial No. 09/178,766, filed October 26, 1998, which is a Divisional of U.S. Patent Application Serial No. 08/734,218, filed October 21, 1996, now USP. No. 6,217,951, the disclosures of which are incorporated herein by reference.

IN THE CLAIMS:

New claims 39-44 have been added as follows:

--39. The method of claim 1, wherein said first voltage is supplied from a first power supply and said second voltage is supplied from a second power supply, said first power supply and said second power supply being separate from one another.

40. The method of claim 7, wherein said first voltage is supplied from a first power supply and said second voltage is supplied from a second power supply, said first power supply and said second power supply being separate from one another.

41. The method of claim 14, wherein said first voltage is supplied from a first power supply and said second voltage is supplied from a second power supply, said first power supply and said second power supply being separate from one another.

42. The method of claim 20, wherein said first voltage is supplied from a first power supply and said second voltage is supplied from a second power supply, said first power supply and said second power supply being separate from one another.

43. The method of claim 26, wherein said first voltage is supplied from a first power supply and said second voltage is supplied from a second power supply, said first power supply and said second power supply being separate from one another.

44. The method of claim 33, wherein said first voltage is supplied from a first power supply and said second voltage is supplied from a second power supply, said first power supply and said second power supply being separate from one another.--